

**REMARKS**

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated March 28, 2005 has been received and its contents carefully reviewed.

In the Office Action, claims 1-8, 10, 12-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,275,061 B1 to Tomita in view of U.S. Patent 6,611,241 B1 to Firester et al and U.S. Patent No. 6,448,952 to Toyoda. Claims 9 and 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tomita in view of Firester and Tododa and further in view of U.S. Patent 5,883,609 to Asada et al. Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Tomita in view of U.S. Patent RE37,847 to Henley et al and Toyoda.

The rejection of claims 1-15 is respectfully traversed and reconsideration is requested. Claims 1-15 are allowable over the cited references in that each of these claims recites a combination of elements including, for example, “said control means controls the scanning driver circuit such that the liquid crystal display panel is scanned in a reverse-sequential manner upon testing of the liquid crystal display panel” (independent claim 1); “setting the scanning lines to a reverse scanning mode” (independent claim 8); “sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing the device” (independent claim 12); and “sequentially scanning the gate lines in a direction identified by the mode setting signal to display a test pattern on the display panel” (independent claim 15). None of the cited references including Tomita, Firester, Toyoda, Asada, and Henley, singly or in combination, teaches or suggests at least this feature of the claimed invention.

The structure of claims 1, 8 and 12 of the present invention are different from the Firester structure in that Firester does not disclose or suggest “the liquid crystal display panel is scanned in a reverse-sequential manner upon testing” as recited in claim 1, “setting the scanning lines to a reverse scanning mode” as recited in claim 8, or “sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing” as recited in claim 12. The Examiner acknowledges that Tomita does not disclose or suggest this feature of the claims, and does not allege that Asada or Henley do.

Firester is directed to a large display comprising an array of smaller display devices or modules and trying to reduce the visual effects along the seams where the various devices abut one another. The Examiner cites a number of passages in Firester that the Examiner asserts

teaches the features of claims 1, 8, and 12 identified above. For example: “Processor 720 processes in parallel 722a, 722b, . . . 722n to interpret the graphics and sub-image data, processes in parallel 724a, 724b, . . . 724n to apply the appropriate correction functions with the sub-image data to compensate for differing brightness levels, registration and focus between image generators and within each image generator, including the pre-distorting and flipping of the sub-images as described above in relation to FIG. 14” (Firester, column 17, lines 43-51) and “Control set-up 910 enables the generation of a test image 912 which is digital image data representing a test pattern, or a sequence of test patterns, that are to be displayed on screen 920. Generator 912 initiates this by (1) applying the test image data to image processor 914 that generates the aforementioned test image and (2) supplying initial or estimated correction factor values to a parameter adjuster 934. The test image is sensed 930, as by a CCD camera or other sensor, and is analyzed 932 with reference to the generated test image 912 to determine errors therebetween.” (Firester, column 19, lines 43-53). Further, Firester states: “Sub-image data inversion is preformed in image processors IP1, IP2, . . . such as by transformation filters that bitmap the pixel data of each sub-image into an addressable random access memory and then read out the pixel data in reverse order, both horizontally and vertically.” These embodiments of Firester are directed to projection displays where an image is projected onto a screen using lenses. The lenses cause the image to be inverted. As a result the image data projected needs to be inverted. That is why Firester discusses “flipping of the sub-images” and reading “out the pixel data in reverse order.” Absent any further specificity in the Office Action, it would seem these are the passages that the Examiner alludes to as teaching these features of claims 1, 8, and 12. This flipping of the sub-image data is different from scanning in a reverse-sequential manner of the present invention. Therefore, Firester does not disclose or suggest “the liquid crystal display panel is scanned in a reverse-sequential manner upon testing” as recited in claim 1, “setting the scanning lines to a reverse scanning mode” as recited in claim 8, or “sequentially supplying the gate signal to the gate lines in a reverse sequential order upon testing” as recited in claim 12. Accordingly, Applicant respectfully submits that claim 1 and claims 2-7, which depend from claim 1; claim 8 and claims 9-11, which depend from claim 8; and claim 12 and claims 13 and 14, which depend from claim 12, are allowable over the cited references.

The structure of claim 15 of the present invention is different from the structure in that Henley does not disclose or suggest “sequentially scanning the gate lines in a direction identified by the mode setting signal to display a test pattern on the display panel” as recited in claim 15.

The Examiner acknowledges that Tomita does not disclose or suggest this feature of the claims, and does not allege that Henley, Asada or Firester do.

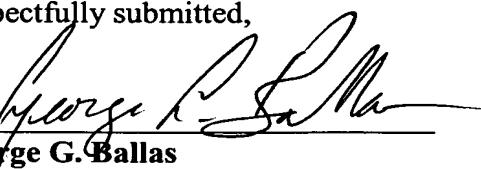
Toyoda is directed to a device for displaying a stereoscopic image in which cross talk is suppressed. As shown in Figure 1, a liquid crystal display is divided into upper and lower regions that are separately scanned in opposite directions. The images in the two different regions are manipulated to create a three dimensional image. The driving circuitry cited by the Examiner in the various cited passages drive the separate regions of the display in opposite or reverse directions. In a given region, the display is scanned in one direction. Data supplied to the display may be reversed, but the scanning is still in a given direction depending upon the portion of the display. (See Toyoda, col. 13, ll. 31-40.) Therefore, this feature of claim 15 is not taught by Toyoda either. Accordingly, Applicant respectfully submits that claim 15 is allowable over the cited references.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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